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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/422,264	04/14/95	GERARDUS DE VRIES	J	P/1034-54

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EXAMINER	
DOLAN,R	
ART UNIT	**PAPER NUMBER**
2306	10

DATE MAILED: 05/09/97

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/422,264	De Vries
Examiner	**Group Art Unit**
Robert J. Dolan	2306

☒ Responsive to communication(s) filed on *Mar 19, 1997* .

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-17, 19, and 21-24* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-17, 19, and 21-24* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☒ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1-17, 19 and 21-24 are presented for examination.

2. The rejection of claim 6 under 35 U.S.C. 112, second paragraph, is withdrawn in view of applicant's amendment.

3. The rejections of claim 5 under 35 U.S.C. 102(b) as being anticipated by Doyle et al, are withdrawn in view of applicant's amendment.

4. The rejection of claim 6 under 35 U.S.C. 102(b) as being anticipated by Cook et al, is withdrawn in view of applicant's amendment.

5. The rejections of claims 1-3 and 7-17 under 35 U.S.C. 103(a) as being unpatentable over Birman in view of Wong and Doyle et al, are maintained and further clarified in view of applicant's amendment.

6. The rejections of claims 4 and 19 under 35 U.S.C. 103(a) as being unpatentable over Birman in view of Wong, are maintained and further clarified in view of applicant's amendment.

Claim Rejections - 35 USC § 112

2. Claims 21-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 21 recites the limitation "the digital data" in lines 3 and 9. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 22 is rejected as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2173.05(l). The omitted structural cooperative relationships are the relationships between the claimed shift register and the apparatus of the independent claim, claim 15.

5. Dependent claims not specifically rejected are rejected as being dependent upon a rejected base claim.15.

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1-3, 7-17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birman in view of Wong et al (Wong) and Doyle et al (Doyle).

Birman teaches a processor comprising:

a multiplier (22) (Fig. 1);

an ALU (20) (Fig. 1);

registers (14) and (16);

a bus structure (18).

Regarding claim 1, Birman does not teach adjustable word lengths in an ALU or a multiplier.

Doyle teaches a data flow component for use as a building block "to provide data flow paths and functions of different data widths for a processor or microprocessor" (lines 3-5 of the abstract). Doyle further teaches that each block may processes virtually any number of bits (line 67 of col. 1 through line 5 of col. 2) and that blocks may be combined to handle wider operands. Thus, the blocks, in essence function as one unit. Further still, Doyle teaches that the blocks are controlled by a processor control unit so as to process bits in any multiple number of the block width (line 63 of col. 5 through line 24 of col. 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Doyle to the apparatus of Birman so as to permit efficient implementation of algorithms, as disclosed by Doyle (abstract).

Wong teaches a multiplier circuit comprised of parallel multiplier units (382), (384), (386) and (388) with associated accumulators. Wong further teaches, in lines 34-41 of col. 2, that the word length of the multiplier may be changed by selectively coupling or decoupling the multiplier units. Although Wong does not explicitly teach operating on words of eight bits, one

of ordinary skill in the art would obviously have been able to extend the teachings of Wong to bit-lengths other than the 16-bit and 32-bit lengths explicitly taught.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Wong to the apparatus of Birman so as to perform both fixed and floating point multiplication, as disclosed by Wong (abstract).

With regard to claims 2, 9 and 16, a pipeline is defined by more than the number of stages or steps it contains. A claim simply of a five-step pipeline without definition of each step does not constitute a patentable difference over the prior art.

With regard to claims 7, 10 and 11, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the circuits in integrated form since it was well known in the art that numerous benefits, such as reduced physical size, exist for integrated circuits.

With regard to claims 8 and 12-15, Birman teaches, in Fig. 2, register file 12, to which separate busses, for example C Bus, from the ALU, and D Bus, from the multiplier, are connected. Further, it was known in the art at the time the invention was made to control bus activity via instruction registers. See, for example Vegesna et al.

With regard to claim 17, it was well known in the art at the time the invention was made to implement Wallace trees in multipliers.

Regarding claim 21, Birman further teaches, in Fig. 2:

a first bus D coupled to the output of the multiplier;

a second bus C coupled to the output of the ALU;

a third bus X and a fourth bus Y coupled to registers (14) and (16).

A fifth data bus coupled to the inputs of the multiplier, the ALU and the register unit is taught as the bus which is coupled to the input of the register (14) and which also bypasses register (14) and connects to the inputs of the multiplier and the ALU via muxes (72), (74) and the unmarked mux coupled to an input of the ALU and the Y bus.

8. Claims 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birman et al (Birman) in view of Wong et al (Wong).

Regarding both claims, Birman does not disclose applicant's claimed adjustable word length in the multiplier. Wong teaches a multiplier circuit comprised of parallel multiplier units (382), (384), (386) and (388) with associated accumulators. Wong teaches, in lines 34-41 of col. 2, that the word length of the multiplier may be changed by selectively coupling or decoupling the multiplier units. Although Wong does not explicitly teach operating on words of eight bits, one of ordinary skill in the art would obviously have been able to extend the teachings of Wong to bit-lengths other than the 16-bit and 32-bit lengths explicitly taught.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Wong to the apparatus of Birman so as to perform both fixed and floating point multiplication, as disclosed by Wong.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle et al (Doyle).

Doyle teaches a data flow component for use as a building block "to provide data flow paths and functions of different data widths for a processor or microprocessor" (lines 3-5 of the abstract). Doyle further teaches that each block may processes virtually any number of bits (line 67 of col. 1 through line 5 of col. 2) and that blocks may be combined to handle wider operands. Thus, the blocks, in essence function as one unit. Further still, Doyle teaches that the blocks are controlled by a processor control unit so as to process bits in any multiple number of the block width (line 63 of col. 5 through line 24 of col. 6).

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (Suzuki) in view of Gergen et al (Gergen).

Suzuki teaches a processor in which data can be left/right shifted a desired number of bits (lines 15-17 of col. 5). Further, Suzuki teaches, in lines 54-67 of col. 5, that a "most significant bit detectors" are used to determine the location of the MSB in each operand. One of ordinary skill in the art would realize that these detectors enable the shifters (14), (15), and (17) to receive data words of variable lengths. Suzuki does not appear to explicitly teach shifting data in a rotating manner.

However, rotating (barrel) shifters were well known in the art at the time the invention was made (lines 21-23 of Gergen et al) and were commonly used in data processing circuits. Such a rotating shifter would have been an obvious substitute for a non-rotating shifter.

11. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Birman in view of Wong et al (Wong) and Doyle et al (Doyle) as applied to claims 1-3, 7-17 and 21 above, and further in view of Suzuki et al (Suzuki) and Gergen et al (Gergen) as applied to claim 6 above.

Regarding claim 22, the combination of Birman, Wong and Doyle does not appear to teach a shifter for shifting/rotating variable length data.

However, as discussed above, the combination of Suzuki and Gergen teaches such a shifter. It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the shifter of Suzuki for that of Doyle ((14) of Fig. 1) in order to prevent overflow and reduce rounding error (lines 13-22 of col. 2 of Suzuki).

Regarding claim 23, Birman teaches, in Fig. 2, a register file (12), to which separate busses, for example C Bus, from the ALU, and D Bus, from the multiplier, are connected. Further, it was known in the art at the time the invention was made to control bus activity via instruction registers. See, for example Vegesna et al.

With regard to claim 24, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the circuits in integrated form since it was well

known in the art that numerous benefits, such as reduced physical size, exist for integrated circuits.

Response to Arguments

12. Applicant's arguments filed 3/19/97 have been fully considered but they are not persuasive.

Regarding claims 1-4, 7-12 and 14-17, applicant has argued that the claimed invention is directed toward a single multiplier and that the Wong reference does not teach such. The Examiner respectfully disagrees. Wong teaches a single multiplier comprising plural multiplier units (382), (384), (386) and (388) with associated accumulators which are appropriately combined to operate on operands of different lengths (abstract). Wong teaches, in lines 34-41 of col. 2, that the word length of the multiplier may be changed by selectively coupling or decoupling the multiplier units.

Applicant has further argued that Wong does not teach operating on words of eight bits or multiples thereof. Although Wong does not explicitly teach operating on words of eight bits, one of ordinary skill in the art would obviously have been able to extend the teachings of Wong to bit-lengths other than the 16-bit and 32-bit lengths explicitly taught. In fact, a "multiple of eight bits" was a common data word increment for data processing.

Further, in the telephone interview on March 4, 1997, the Examiner suggested to applicant's representatives that Fig. 7 of the application shows a multiplier similar in

construction to that of Wong. Applicant has responded that the claimed multiplier is "merely schematically represented" in Fig. 7. The Examiner would like to point out that the specification states, in line 33 of page 6 through line 1 of page 7, that "All possible multiplication operations .. is possible, inter alia due to the presence of a Wallace tree (fig.7)," apparently indicating that Fig. 7 is more than a mere "schematic representation."

Regarding claim 5, applicant has argued that the claimed invention is directed toward a "single ALU" and that such is not taught by the Doyle reference. However, Doyle clearly states, in lines 12-16 of the abstract, that the blocks may be used in combination to implement arithmetic algorithms. Even if one does not consider that an ALU is, in itself, some combination of building blocks, the system taught by Doyle is at least functionally equivalent to the claimed invention.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert J. Dolan whose telephone number is (703) 305-2875. The examiner can normally be reached on M-F from 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reba I. Elmore, can be reached on (703) 305-9706. The fax number for the group is (703) 305-9724.

Robert J. Dolan
Patent Examiner
Art Unit 2306

REBA I. ELMORE
PRIMARY EXAMINER
GROUP 2300

May 5, 1997